GENERAL FRONT END ARCHITECTURE

ANALOG | DIGITAL

~100

| AGC | A/D | EQUALIZER | INTERP |

112   110

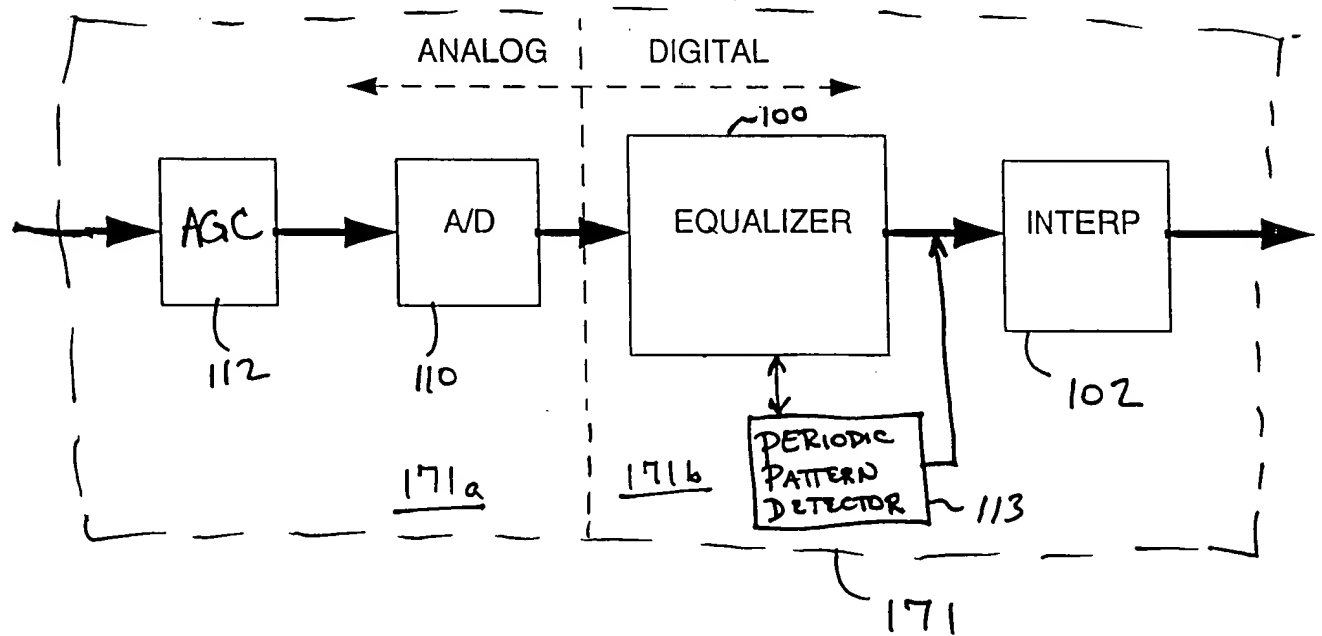171a   171b

PERIODIC PATTERN DETECTOR ~113
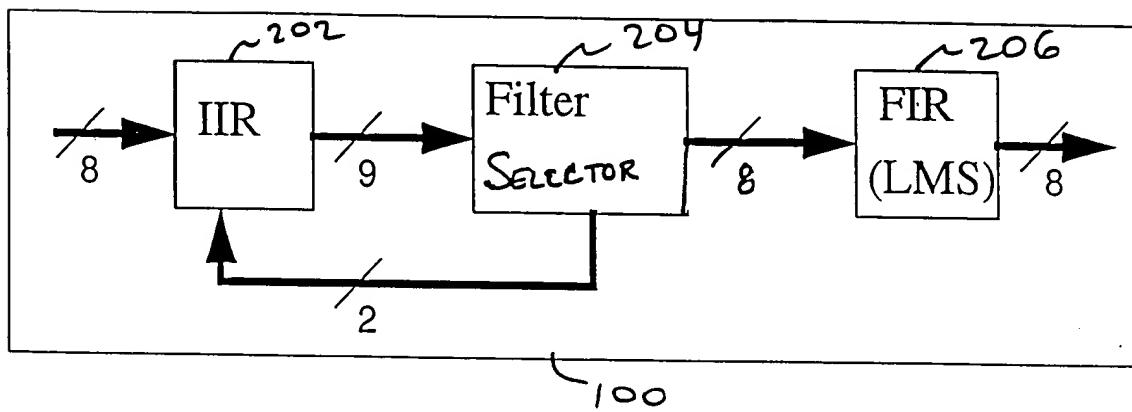
102

171

FiG. 1

EQUALIZER ARCHITECTURE

FIG. 2

IIR Filter Block Description

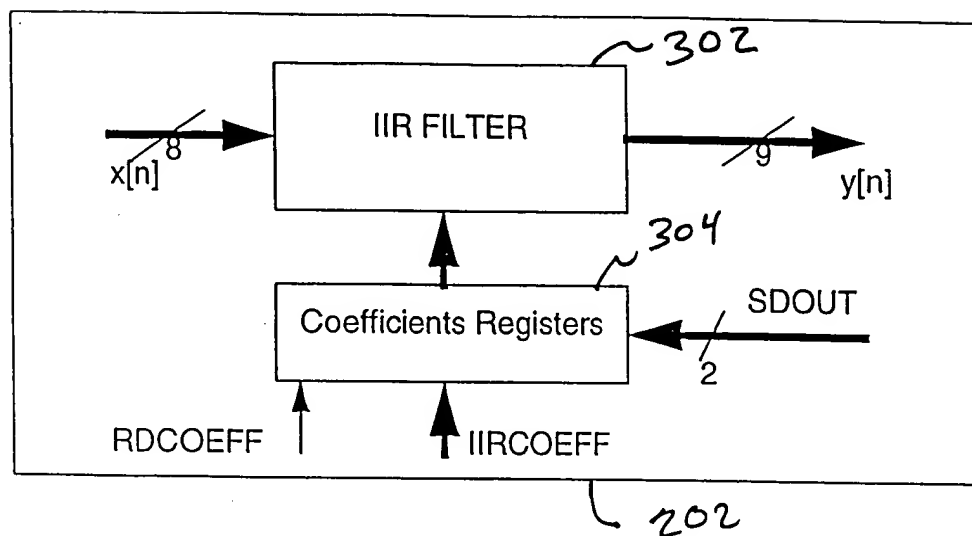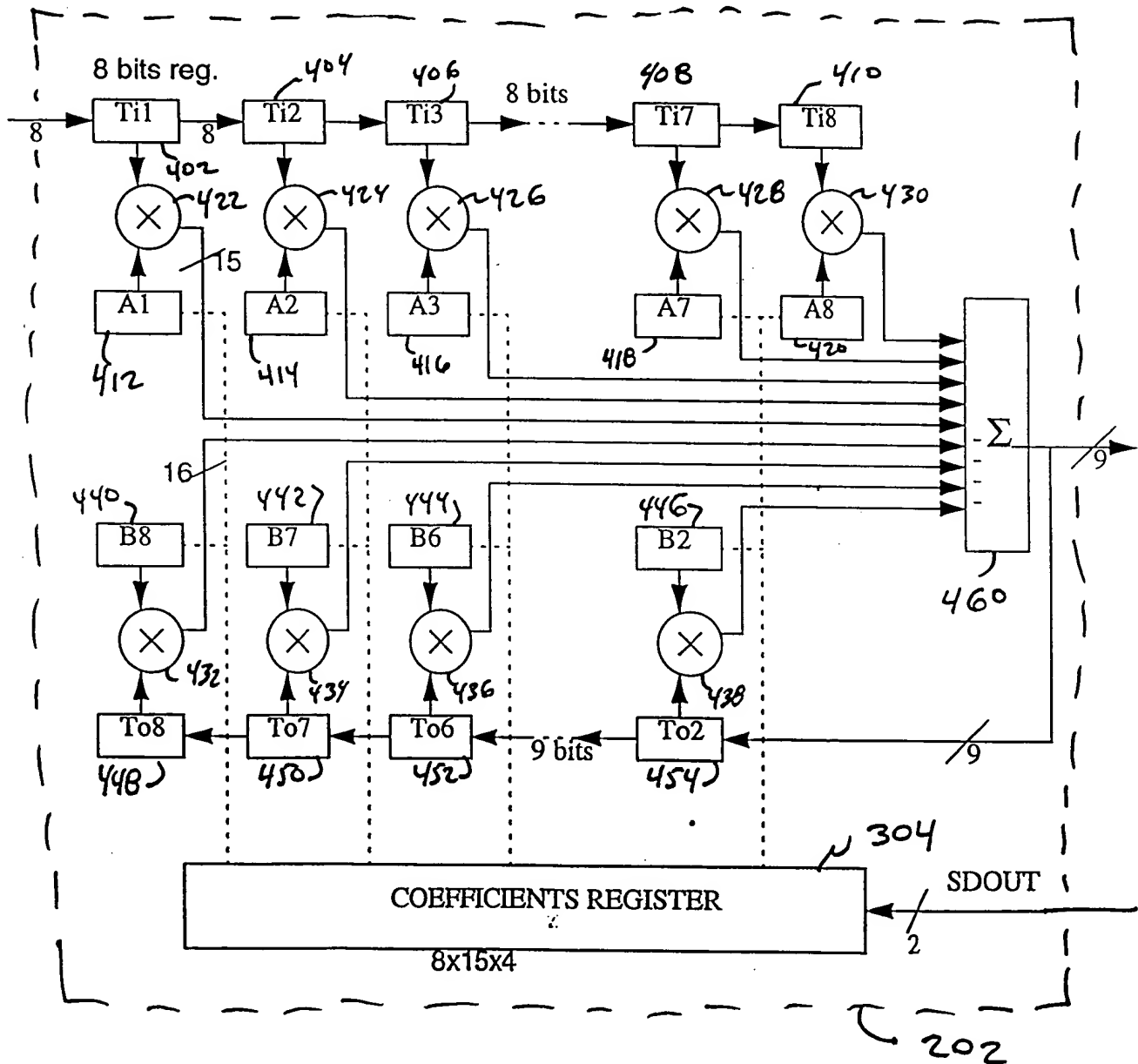
FIG. 3

IIR Filter Block Implementation
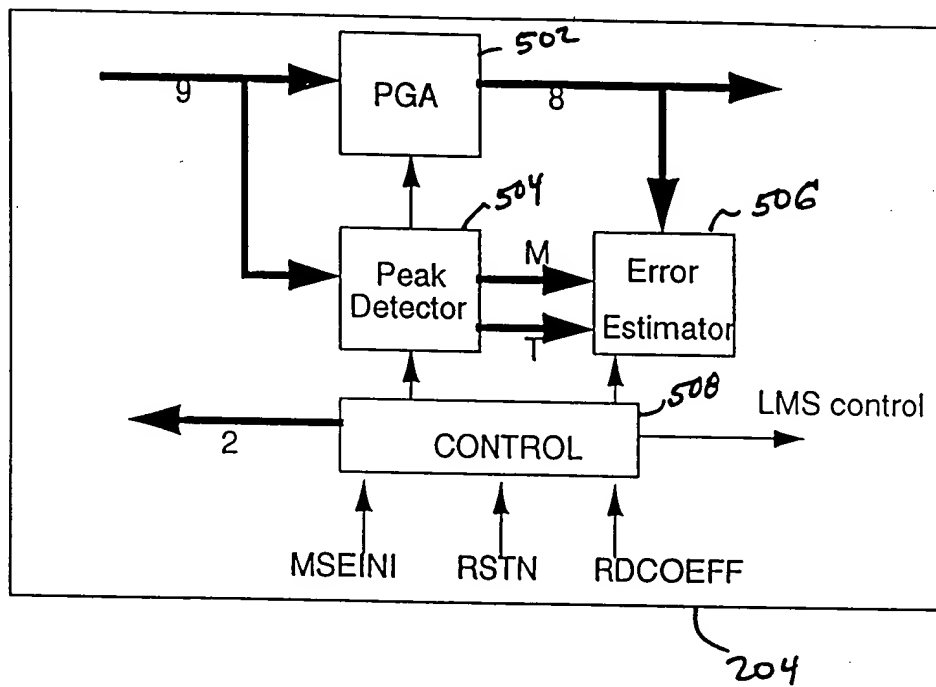

FIG. 4

Filter Selection Block Description

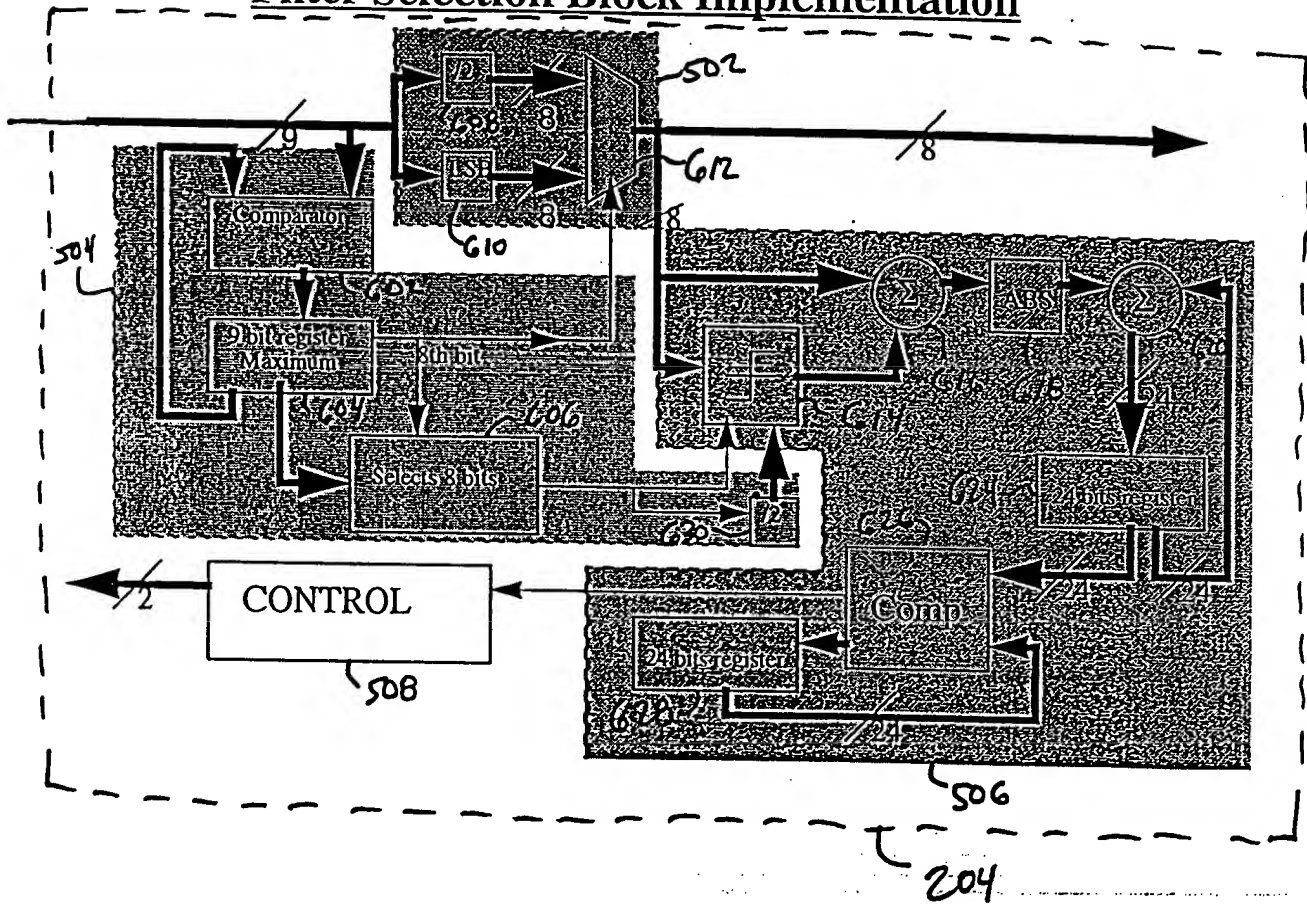

FIG. 5

Filter Selection Block Implementation

F.G. 6

Adaptive FIR Filter Description

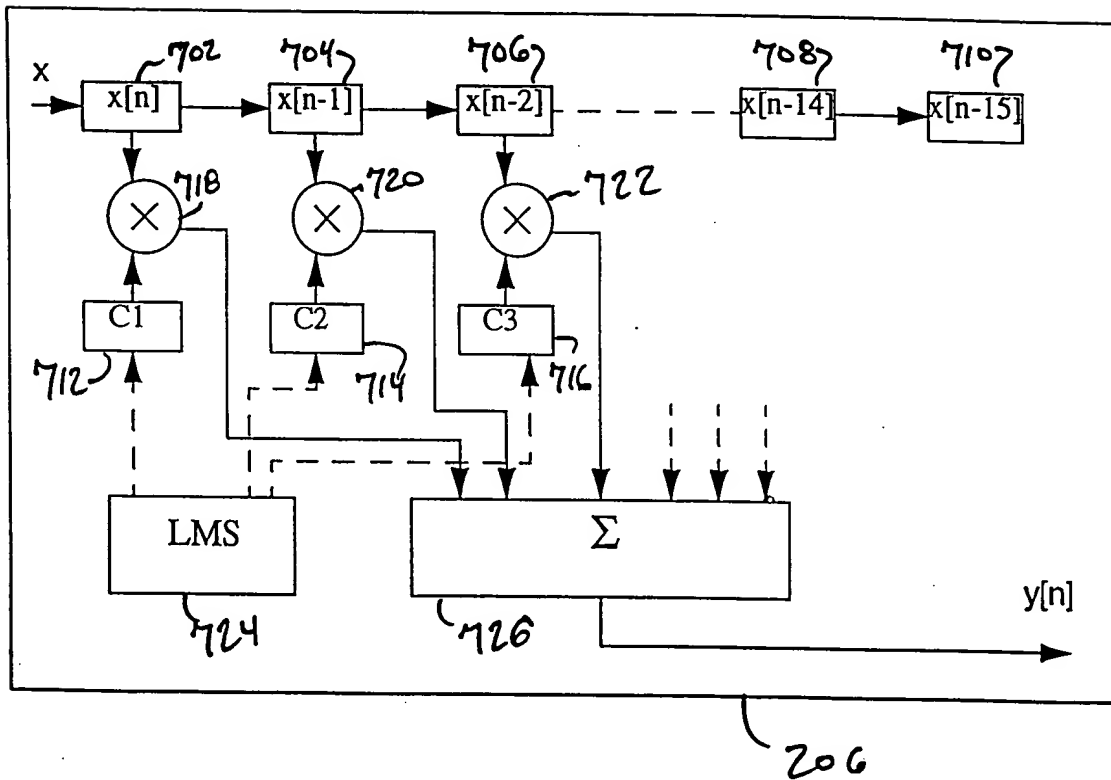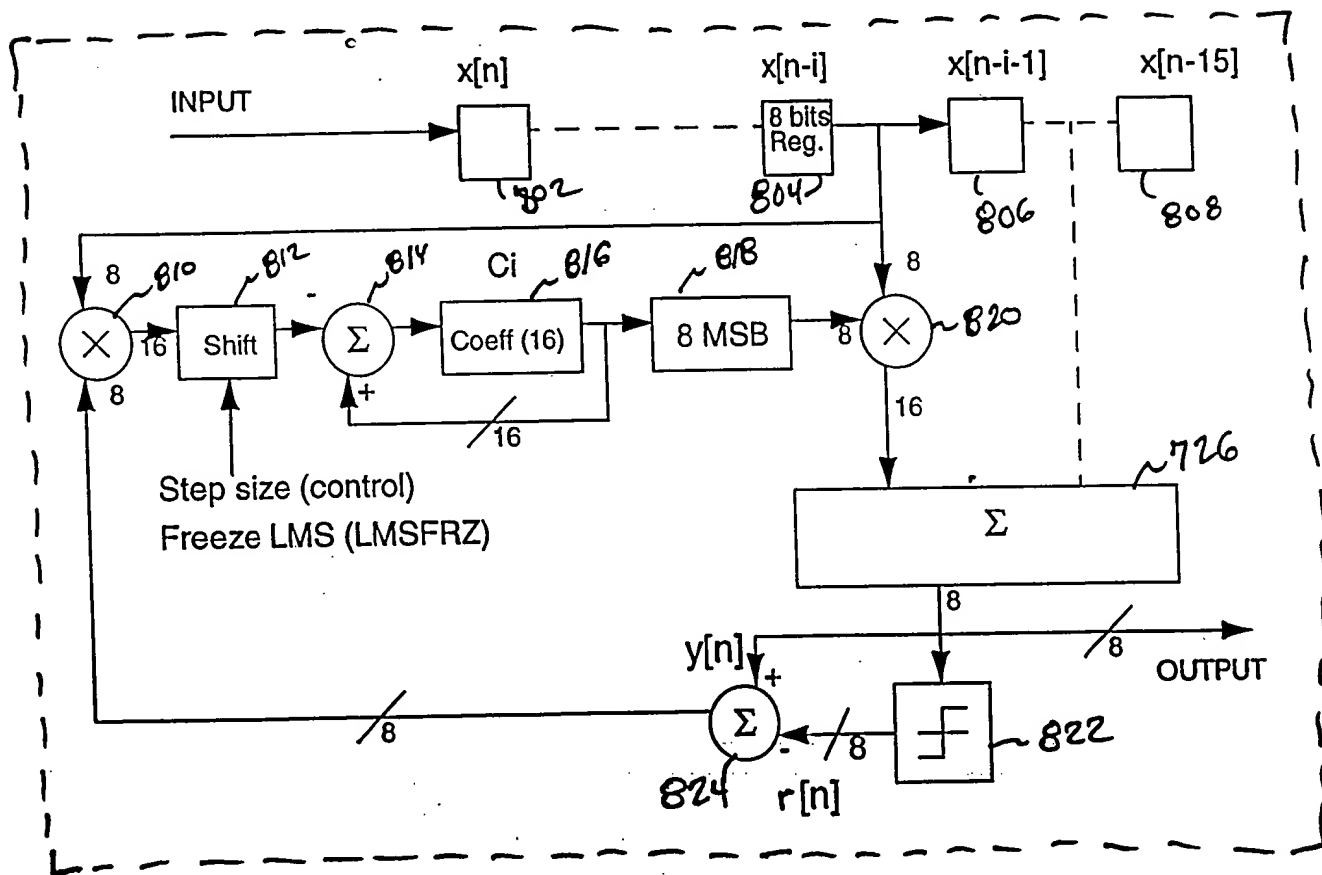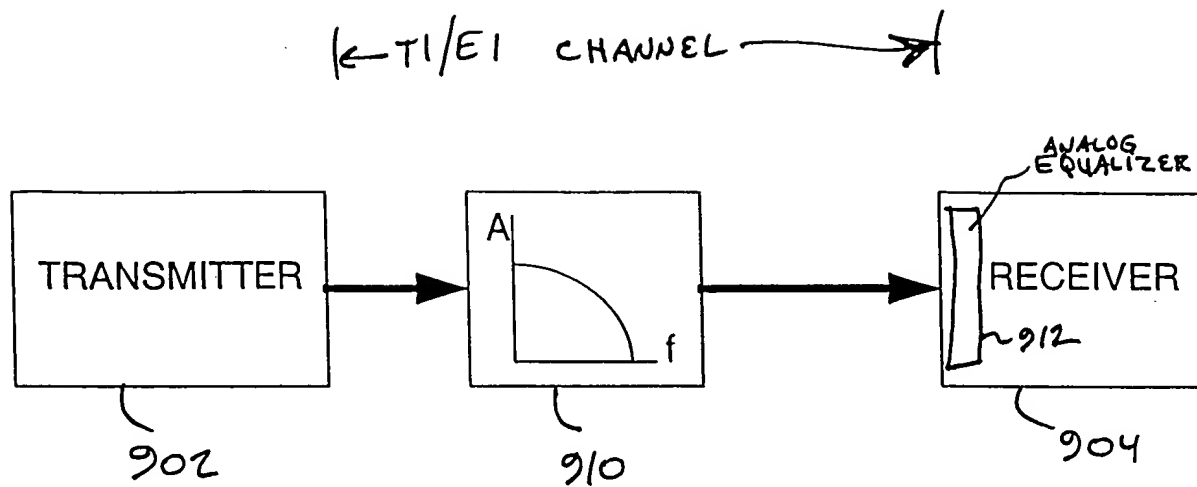FIG. 7

Adaptive FIR Filter Block Implementation

FIG. 8

←— TI/EI CHANNEL —→

TRANSMITTER

902

A
f

910

ANALOG
EQUALIZER

RECEIVER

912

904

PRIOR ART

FIG. 9